Radiation Hardness Evaluation of a Class V 32-Bit Floating-Point Digital Signal Processor

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ABSTRACT

The Single Event Effects (SEE) and Total Ionizing Dose (TID) test results of SMV320C6701, a 32-bit, floating-point digital signal processor (DSP) from Texas Instruments (TI) are reported in this paper.

The DSP was tested for SEE using heavy ions and high energy neutrons. Effects characterized include Single Event Upsets (SEU) and Single Event Latch-up (SEL). Additional effects such as functional interrupts and transients are also discussed. Finally, the proton SEU rates extrapolated from the heavy ion SEU rates are presented.

I. INTRODUCTION

Large amount of data processing and movement is required on a spacecraft which is generated by numerous sensors on board. A high speed, floating-point DSP can optimally handle this demanding task of data processing if it remains uninterrupted by the effects of radiation.

One such DSP being considered for future space applications is a Class V offering from Texas Instruments, the SMV320C6701 [1]. Therefore, an in-depth study of the TID and SEE response of this DSP was undertaken.

II. BACKGROUND

In order to become familiar with this DSP, its primary features are briefly reviewed. The parent device is the TMS320C6701 DSP which has been offered in the commercial marketplace since 1998. It is the first and only DSP family to natively support both single- and double-precision IEEE floating-point operation in hardware. In addition, the processor is fully upward compatible with the TMS320C6201 and its family of fixed-point processors. The processor is implemented in a 0.18-µm, five-level metal, CMOS process. This overview of the SMV320C6701 will include the core CPU, onboard memory the DMA controller and on-chip peripherals as shown below in Figure 1.

The CPU consists of eight independent functional units each of which can process a 32-bit instruction every clock cycle. TI applies the term VelociTI™ to describe this advanced variation of a traditional VLIW (Very Long Instruction Word) architecture. Since the SMV320C6701 operates at a 140-MHz clock rate, this means that the CPU can process up to 1,120 million instructions per second. The instruction set architecture is RISC-like and register based meaning that the source and destination operands of nearly all instructions are located in the register file. Six of the eight functional units are capable of performing a floating-point operation every clock cycle. The processor is capable of performing two IEEE single-precision, multiply-accumulate operations every clock cycle. The instruction set was designed to make the processor an excellent target for a C compiler. Memory is byte addressable, and load/store instructions support moving
8-, 16- and 32-bit data. Two of the core's eight functional units support simultaneous memory accesses each cycle.

On-chip memory includes one megabit of SRAM. This memory is organized into a Harvard-style architecture where program and data memory reside at different addresses. The memory is equally divided between the program space and the data space, so 64K bytes are available to each. The program space allows holding 16K 32-bit instructions. As an alternative, the program memory can be enabled as an on-chip cache to improve effective access time to external memories. The data memory supports dual accesses in a single cycle.

VelociTI is a trademark of Texas Instruments Incorporated.

Portions of this paper were presented at CMSE Europe 2004.

This allows the two load/store functional units to have unrestricted access to internal memory.

To facilitate movement of data in parallel with other CPU operations, the processor has a Direct Memory Access (DMA) controller that provides four channels. Transfers can free run in a cycle-stealing mode or be synchronized on reads, writes, or both. Arbitration priority with the CPU is selectable. The DMA is capable of bootloading the processor on reset. It also has a dedicated fifth channel that is hardwired to the SMV320C6701 Host Port. The DMA can read tables of configuration information stored in an on-chip “parameter RAM” that allow it to reprogram itself after a transfer without CPU intervention. This reduces or eliminates the need to have the CPU involved in managing the DMA controller.

The SMV320C6701 includes a rich set of onboard peripheral devices. The External Memory Interface (EMIF) allows glueless connection to asynchronous memories (SRAM, EPROM) and synchronous memories (SDRAM, SBSRAM). The EMIF is supported by four independent sets of control signals allowing mixing of four types of memory in the system without the need for additional external decoding. The EMIF allows accessing 52 megabytes of external memory.

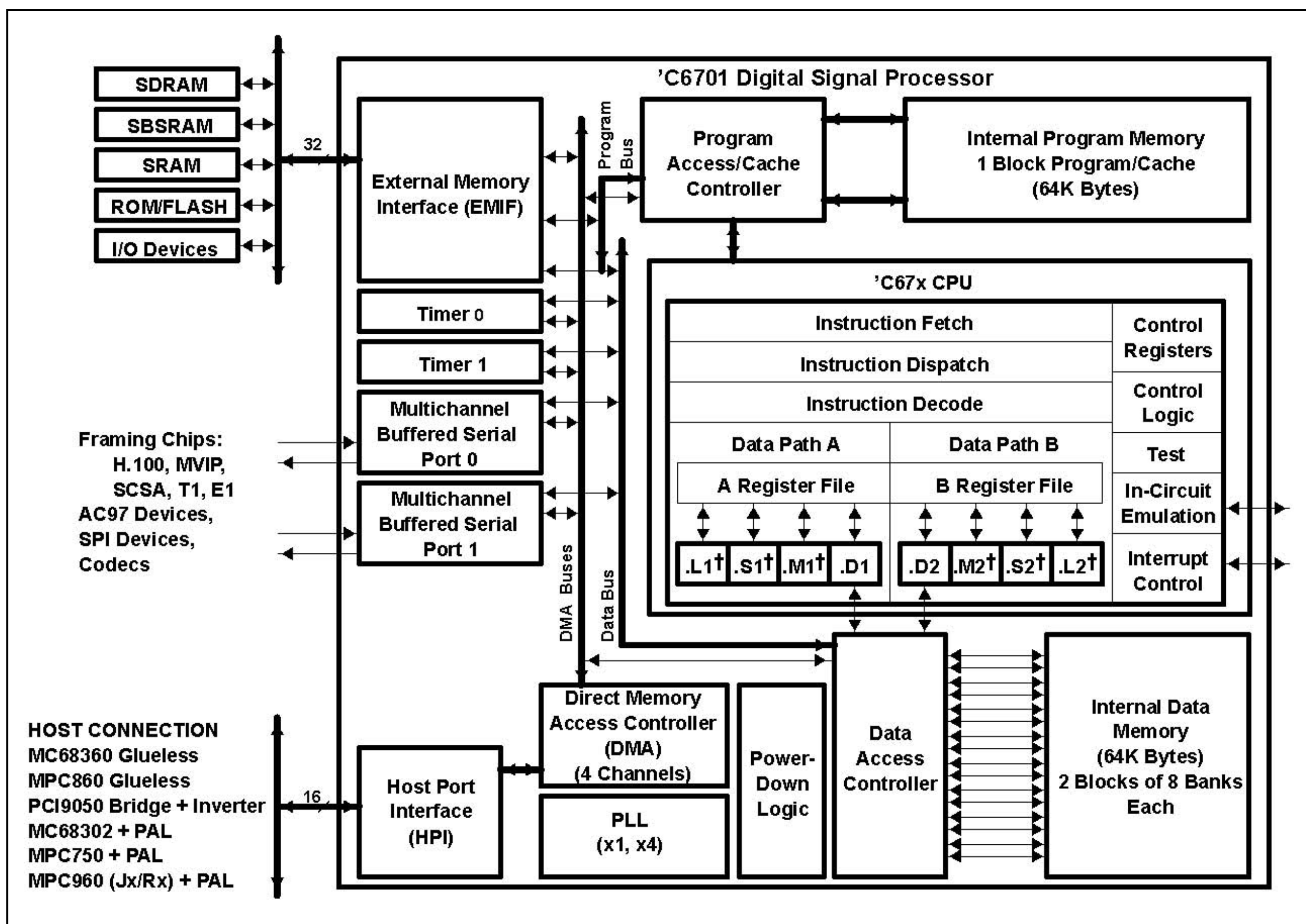

Figure 1. C6701 Functional Block Diagram

The Host Port Interface (HPI) provides a 16-bit bus for connection to an external processor. The interface supports glueless connection to a wide variety of available microcontrollers. Through the HPI, a host processor is able to access the entire memory map of the DSP whether the location is an on-chip or off-chip address. The processor includes two Multichannel Buffered Serial Ports (McBSPs). These serial ports provide a glueless connection to T1/E1, MVIP and SCSA framer chips. They support the ST-Bus switching protocol. They can be operated in a time-division mode that supports up to 256 channels per serial port. The serial ports are full duplex and can operate with independent transmit and receive clocks and frame sync signals. Finally, the serial ports also support the Serial Peripheral Interface (SPI) protocol.

The SMV320C6701 has two on-board, general purpose, 32-bit timers capable of being driven from an internal or external clock source. The processor also includes a flexible phase-locked loop (PLL) generator that allows running the processor from a low frequency input clock. Finally, the processor features an IEEE-1149.1 JTAG standard Test Access Port that can be used for test and emulation purposes.

The processor is available in a 429-pin, dimpled ceramic, ball grid array package (GLP suffix) that is pin compatible with the MIL-PRF-38535 Class Q SMJ320C6701. The processor requires a dual power supply. The I/O operates at 3.3 V while the core of the processor operates at 1.9 V. The operating temperature range is from -55°C to 125°C (Tcase).

III. TEST DEVICE

SMV320C6701GLPW14 (5962-9866101VXA) was the Device Under Test (DUT) for all of the radiation exposure testing. Since this device is available in a flip-chip package, for heavy ion testing, the devices were de-lidded and the substrate was etched to 70 µm to allow the heavy ions to reach the sensitive regions of the device.

Table I lists the key features of the DUT. It should be noted that the epitaxial layer is the process baseline for the Class V offering of C6701 which is crucial for an enhanced SEL performance.

Table I. C6701 Key Features

<table>
<tr><th colspan="2">Design Features</th><th colspan="2">Process Features</th><th colspan="2">Library Features</th></tr>
<tr><td>Core Vdd</td><td>1.9 V</td><td rowspan="2">Starting Substrate (Baseline for Class V)</td><td rowspan="2">Epitaxial 3.5 µm</td><td>Metal Levels</td><td>5</td></tr>
<tr><td>IO Vdd</td><td>3.3 V</td><td>Flip Chip</td><td>Yes</td></tr>
<tr><td>Core Lpoly</td><td>0.18 µm</td><td rowspan="4">Shallow Trench Isolation (STI) Depth</td><td rowspan="4">5000 Å</td><td rowspan="4">PLL</td><td rowspan="4">Yes</td></tr>
<tr><td>Core tox</td><td>40 Å</td></tr>
<tr><td>IO Lpoly</td><td>0.45 µm</td></tr>
<tr><td>IO tox</td><td>80 Å</td></tr>
</table>

Note: 1 Å = 0.1 nm

IV. TOTAL IONIZING DOSE

A. Test Procedure

The total dose testing was performed in accordance with MIL-STD-883E, Method 1019.6. The irradiator was "JL Shepard Gammabeam 150-C" room source at the Salk Institute, San Diego, CA. The DUTs were subjected to a minimum of 32 hours of burn-in at 150°C to exclude any devices with potential reliability defects. There were seven groups, of five devices each that were subjected to gamma radiation. The dose rate was 1.7 rad(Si)/second. With one irradiation level for each group, the seven irradiation levels used were 40, 50, 60, 70, 100, 150 and 200 krad(Si). The devices were biased, but in static mode, at the time of radiation exposure. Functional and parametric verification of the devices was done pre- and post-radiation exposure. This verification was performed at two supply voltages of 3.14 V and 3.46 V using Texas Instruments "V-Series" Automatic Test Equipment (ATE). Functional verification included test coverage of all the major blocks shown in Figure 1. Parametric verification included timing, voltage and current measurements in accordance with the Standardized Military Drawing (SMD) 5962-986610. Pre- and post-irradiation deltas were calculated on a per device basis on a total of 214 test parameters organized by group. These groups were subjected to an ANOVA analysis. ANOVA stands for "Analysis of Variance" and is used to indicate when statistically significant differences exist between groups of data.

B. Test Results

For every device from 40-, 50-, 60-, 70-, 100-krad(Si) groups, the ANOVA analysis indicated that there were very few device parameters which exhibited any statistically significant difference. For each parameter, the maximum observed delta was compared against the ATE resolution to indicate whether the deltas could be considered to be significant. In every case, the maximum delta observed was well within the resolution of the ATE, so no inferences could be made from the differences that were observed.

All devices subjected to 150 kad(Si) exhibited tri-state leakages on multiple pins. However, they remained functional. The devices subjected to 200 krad(Si) were non-functional showing internal supply shorting along with exhibiting tri-state leakage on multiple pins.

V. HEAVY IONS

A. Test Procedure

Heavy ion testing was performed at the Texas A&M University's Cyclotron facility using a K500 Superconducting Cyclotron accelerator. The effective linear energy transferred (LETeff) of heavy ions used for this test ranged from 6.24 to 89 Mev-cm^2/mg. Table II lists the heavy ion species used for the test with respective LETeff, the number of units tested at a particular LETeff and the test temperature. The devices were maintained at room temperature (approximately 25°C) at lower LETeff tests and elevated temperature of 125°C during high LETeff tests.

The devices were tested in dynamic mode and were exercised using Texas Instruments "VLCT", a 256-pin ATE. The VLCT was controlled by a SUN SPARC workstation using Tester Programming Language (TPL) for monitoring and issuing commands to the DUT. The TPL was developed to provide the capability of monitoring the device currents for I/Os, Core and PLL for latch-up throughout testing. The TPL was designed such that it could issue commands to the ATE for a power-down of the DUT when device currents exceeded its normal levels indicating latch-up conditions and thus protect the DUT from electrical overstress.

Table II. Ion Species and LETeff

Ions	Incident Angle	LETeff Mev-cm^2/mg	#Units	Test Temperature
Ar	0°	6.24	1	25°C
Ar	45°	9.16	2	25°C
Kr	0°	23.6	2	25°C
Kr	45°	35.4	2	25°C
Xe	0°	47.1	1	25°C
Xe	45°	71.1	1	25°C
Xe	45°	71.1	3	125°C
Xe	45° + #2 Degrader	89	3	125°C

The VLCT is an event-driven tester with functional and SCAN test capability along with the capability to log parametrics and fail counts. The test suite was developed using TPL for verification of all the major functional blocks described in Figure 1. The test suite consisted of 24 different test types exercising different functional blocks of the device at different bias voltage combinations. Each test type consisted of several test vectors that ranged from several thousand to several million. The DUT was exercised with test vectors at a translated frequency of ~10 MHz. In addition to functional testing, the on chip SRAM was tested using internal Built-In-Self-Test (BIST). This BIST verification was performed at 167 MHz.

The test flow started with a DUT continuity check, followed by exercising the DUT with test vectors and monitoring device currents for a SEL. If no SEL occurred, then a looping of the test vectors was performed as fluence levels increased, and functional fail counts were recorded for SEE. The full test suite was run at multiple voltage bias conditions at every LETeff listed in Table 2. The voltage bias conditions ranged from 2.35 V to 3.63 V for I/Os and 1.4 V to 2.05 V for core.

B. Test Results

With the help of functional fail counts and fluence level for the respective test, the SEU characteristics of different functional blocks of the DUT were calculated. Figures 2 to 5 show the SEU characteristics of different functional blocks in terms of cross-section vs. LETeff at room temperature. The results of the SEU tests were analyzed using Weibull curve fitting parameters and upset rates were estimated using CREME96 model [2] for the galactic cosmic ray background environment (solar minimum and maximum conditions) and for an Anomalously Large Solar Flare (ALSF).

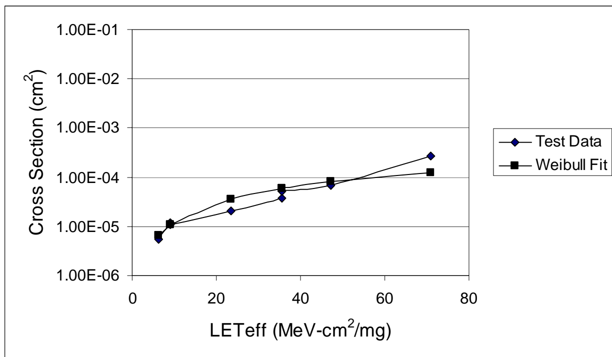

Figure 2. SEU Characteristics - EMIF, McBSP, DMA, Power Down Logic, Data Access Controller, Program/Cache Memory, Data Memory, Boot Modes

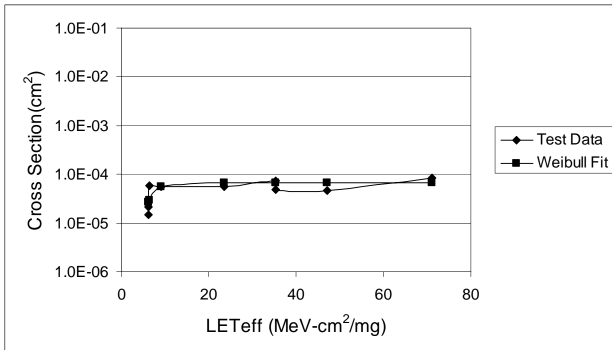

Figure 3. SEU Characteristics - Program/Cache and Data Memory, Program Access/Cache Controller and Data Access Controller

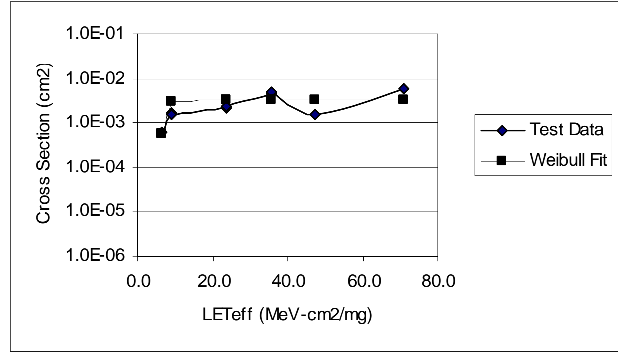

Figure 4. SEU Characteristics – Data Memory Verification using BIST

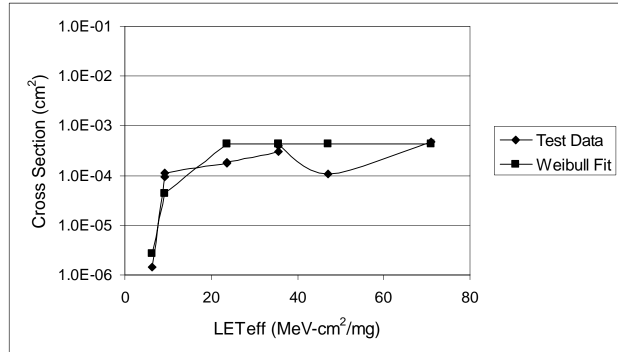

Figure 5. SEU Characteristics - CPU

Table III. Summary of Weibull Fit Parameters for SMV320C6701

CREME96 Input (Weibull Parameters)	EMIF, McBSP, DMA, Power Down Logic, Data Access Controller, Program / Cache Memory, Data Memory, Boot Modes	Program / Cache and Data Memory Program Access/Cache Controller and Data Access Controller	Data Memory Verification using BIST	CPU
Onset	0.200	0.700	6.239	3.627
WL	99.0	9.000	16.402	0.100
Pwr	2.0	3.000	0.234	1.514
Length	1.79	6.988	47.33	6.222616
Width	10.58	2.329	12.71	0.997549
Height	2	1	5.4	2.458734
Asymptote	1.9E+01	1.628E+01	6.0E+02	6.207E+00
# Bits	2.0E3	400	500	2.00E+03

Table IV. Summary of the SEU Rates (Upsets/day) for the SMV320C6701

Environment	EMIF, McBSP, DMA, Power Down Logic, Data Access Controller, Program / Cache Memory, Data Memory, Boot Modes	Program / Cache and Data Memory Program Access/Cache Controller and Data Access Controller	Data Memory Verification using BIST	CPU
solar min	4.11E-05	3.32E-04	6.39E-03	7.94E-04
solar max	9.17E-06	6.83E-05	1.12E-03	1.13E-04
worst 5-min	3.78E-02	2.44E-01	1.80E-02	5.83E-01
worst day	3.59E-04	2.43E-03	1.44E-00	5.40E-03
worst week	1.85E-04	1.42E-03	3.4E-00	3.79E-03

The Weibull fit parameters derived from the test data for the various functional blocks and SRAM are shown in Table III. Table IV is a summary of upset rates for the DSP. The DSP has an average background SEU rate of 7.6E-03 upsets/device-day or ~130 days per upset (GEO orbit). The average ALSF upset rates are shown in Table V.

Table V. Average ALSF Upset Rates

Environment	Device Upset Rate (upsets/device-day)
Worst 5-min	8.83E-01
Worst day	1.45E-00
Worst week	3.41E-00

VI. PROTON UPSET RATE ESTIMATIONS

The proton upset rates for various LEO orbits are estimated using the heavy ion test data. At the time of the latest document revision, additional third-party proton radiation exposure results were made available. Please reference the paper: D.M. Hiemstra, B. Miladinovic and F. Chayab, "Single Event Upset Characterization of the SMJ320C6701 Digital Signal Processor Using Proton Irradiation," to be published in IEEE REDW 2005.

Proton upset cross section vs. energy was calculated from the heavy ion upset cross section vs. LETeff using approaches derived by J.G Rollins [3] and further complemented by E.L. Peterson [4].

Both the approaches have inherent uncertainty. Nevertheless, they can be used to give rough order of magnitude (ROM) upset rates. Trapped protons are the primary cause of single event upset in low-earth orbits (LEO). The environmental proton flux for various orbits was derived using the NASA AP8 models [2] [5].

The AP8 trapped proton models are empirical models of the omni directional trapped proton flux in earth's magnetosphere. The models were derived from measurements accumulated by numerous satellites in the 1960s and 1970s. Although the AP8 models are now more than 20 years old, they are still the most comprehensive trapped proton models available. Due to changes in the geomagnetic field, the AP8 models no longer provide reliable maps of the geographic distribution of trapped protons. Nevertheless, comparisons with on-orbit dose and SEU observations suggest that these models generally provide omni- directional, orbit-averaged quantities which are accurate to within a factor of two.

Upset rates were calculated using the integral method. The upset rate is the sum of the differential average daily flux integrated over the cross section vs. energy. Upset rates for various functional blocks of the DSP estimated for the different LEO orbits are shown in Tables VI to VIII.

The estimated upset rate for the Space Station Orbit is 4.9E-5 upsets/device-day or ~56 years per upset. For the Shuttle Orbit the upset rate is estimated to be 6.9E-5 upsets/device-day or ~39 years per upset.

Table VI. Proton Upset Rates (Upsets/day) at Various Altitudes and 0 deg. Inclination Angle

Functional Block	1,000 km	5,000 km	10,000 km	15,000 km
Data Memory Verification using BIST	1.6E-04	1.7E-01	2.0E-02	1.9E-05
CPU	1.03E-07	8.04E-05	3.97E-06	7.90E-11
Program/Cache and Data Memory Program Access/Cache Controller and Data Access Controller	1.77E-06	3.54E-03	2.15E-04	2.07E-07
EMIF, McBSP, DMA, Power Down Logic, Data Access Controller, Program/Cache Memory, Data Memory, Boot Modes	2.75E-06	6.76E-03	4.11E-04	3.95E-07

Table VII. Proton Upset Rates (Upsets/day) at Various Altitudes and 28.5 deg. Inclination Angle

Functional Block	1,000 km	5,000 km	10,000 km	15,000 km	SHUTTLE 450 km 28.5 DEG
Data Memory Verification using BIST	7.9E-04	8.4E-01	4.8E-02	5.8E-05	1.1E-05
CPU	2.38E-06	4.05E-05	1.54E-06	2.91E-11	1.03E-07
Program/Cache and Data Memory Program Access/Cache Controller and Data Access Controller	8.58E-06	9.14E-03	5.28E-04	6.33E-07	1.04E-07
EMIF, McBSP, DMA, Power Down Logic, Data Access Controller, Program/Cache Memory, Data Memory, Boot Modes	6.51E-05	1.05E-03	8.15E-05	1.46E-07	5.79E-05

Table VIII. Proton Upset Rates (Upsets/day) at Various Altitudes and 51.6 deg. Inclination Angle

Functional Block	1,000 km	5,000 km	10,000 km	15,000 km	SPACE STATION 500 km 51.6 DEG
Data Memory Verification using BIST	9.0E-04	4.6E-01	4.4E-03	4.1E-06	4.6E-05
CPU	1.39E-06	2.20E-05	8.71E-07	1.70E-11	1.27E-07
Program/Cache and Data Memory Program Access/Cache Controller and Data Access Controller	9.85E-06	5.06E-03	4.77E-05	4.45E-08	1.28E-07
EMIF, McBSP, DMA, Power Down Logic, Data Access Controller, Program/Cache Memory, Data Memory, Boot Modes	3.91E-05	5.90E-04	9.11E-05	8.50E-08	2.75E-06

Table IX. High Energy Neutron – SEL Test Conditions and Results

	Temperature	Exposure Time (hours)	Flux (neutrons/cm^2/hr)			Latch-up Free Operation Equivalency (years)	
			Beam	Sea -level	40 k feet	Sea -Level	40 k feet
DUT1	25°C	4.5	1.41E+10	20	5016	3.63E+05	1.45E+03
	125°C	0.75	2.74E+09	20	5016	1.17E+04	4.68E+01
	25°C	11.75	3.13E+10	20	5016	2.10E+06	8.37E+03
DUT2	125°C	8	2.30E+10	20	5016	1.05E+06	4.19E+03
DUT3	25°C	8	2.20E+10	20	5016	1.01E+06	4.01E+03
	125°C	7.75	1.92E+10	20	5016	8.49E+05	3.39E+03
DUT4	125°C	13	3.46E+10	20	5016	2.56E+06	1.02E+04

VII. HIGH ENERGY NEUTRONS

A. Test Procedure

The high energy neutrons latch-up testing was performed at "The Los Alamos Neutron Science Centre", Los Alamos, NM. The 800 MeV Proton Linear Accelerator was the energy source and U^{238} Fission foil was used for the upper level counts. Four DUTs were tested for SEL at 125°C. The supply currents and signature for functional failures were monitored throughout the testing.

B. Test Results

There was no SEL observed on any of the four DUTs. Table IX shows for every DUT the temperature, exposure time and the neutron flux for the beam during the test. Also shown are the neutron flux at sea-level and 40k feet. Using the beam neutron flux and the exposure time, the total number of neutrons that the DUT was exposed is calculated. This is then used in determining a latch-up free operation for the DSP in terms of number of years both at sea-level and 40,000 feet.

VIII. LIMITATIONS

The authors would like to discuss some limitations experienced during the irradiation testing of this DSP. The heavy ion testing was performed using a production ATE and production test suite. This allowed exhaustive functional testing of various functional blocks of the DSP. However, due to the complexity of the DSP, its Harvard-style architecture and test methodology, it was an impossible task to isolate Single Event Functional Interrupts (SEFI) from SEU. As a worst case, the SEFI rate could be expected 7.6E-03 upset/device-day from the test results of SEU. Single Event Transients (SET) can cause upsets in flips-flops when they propagate to the data input of the flip-flop near the clock edge. Testing at low frequency can hide the severity of the problem. Therefore, as a future work, evaluation of SEFI and SET with high frequency testing using an application board is proposed.

The BIST algorithm used to obtain the SRAM SEU data for both the Program and Data memory is not representative of SRAM behavior in a typical system. Since this algorithm is designed to be an efficient manufacturing test, it contains attributes that make it non-ideal for evaluating SEU rates. It is recommended that SEU data be obtained utilizing a test that is representative of intended system application.

The BIST results for Program memory have been removed from the analysis due to errors that cause results to appear overly optimistic. Physical construction of Data and Program memories are identical. Data memory SEU results can provide relative performance of Program Memory.

Due to hardware and software limitations at the time of high energy neutrons test, it was not possible to determine SEU rates.

IX. CONCLUSIONS

The minimum Total Gamma Dose tolerance of the SMV320C6701 is 100 krad(Si). The thin gate oxide both for the core and I/Os resulted in fewer oxide trapped charges and lower Vt shift. However, Radiation Induced Leakage Currents (RLIC), due to trapped assisted tunneling, manifested as tri-state leakage failures.

The DSP is not susceptible to SEL up to tested LET of 89 MeV-cm^2/mg and max temperature of 125°C. The thin epitaxial layer, which is the process baseline for the Class V DSP, contributed to this excellent SEL performance. The DSP has an average background SEU rate of 7.6E-03 upsets/device-day or ~130 days per upset (GEO orbit) when tested with heavy ions. The DSP was not sensitive to bias voltage or temperature.

The proton upset rates for various LEO orbits were estimated using the heavy ion test data. The estimated upset rate for the Space Station Orbit is 4.9E-5 upsets/device-day or ~56 years per upset. For the Shuttle Orbit the upset rate is estimated to be 6.9E-5 upsets/device-day or ~39 years per upset. At the time of latest document revision, additional third-party proton radiation exposure results were made available. As mentioned above, please reference the paper: D. M. Hiemstra, B. Miladinovic and F. Chayab, "Single Event Upset Characterization of the SMJ320C6701 Digital Signal Processor Using Proton Irradiation," to be published in IEEE REDW 2005.

SEL was not observed on any of the devices when tested with high energy neutrons at 125°C.

The minimum TID tolerance of 100 krad(Si) and very low non-SRAM susceptibility to SEE makes SMV320C6701 a suitable candidate for various LEO, GEO and avionics applications with proper mitigation.

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REVISION HISTORY

7/02/2005: Revised heavy ion and proton SEU rates based on updated Data memory SRAM results. SRAM results for Program memory were removed due to inability to detect bit errors in majority of test runs.

REFERENCES

[1] SMJ320C6701 Product Datasheet Texas Instruments SGUS030B 5/01
[2] IEEE Trans. Nucl. Sci. vol 44, No. 6 pp 2150 – 2160, Dec. 1997 https://creme96.nrl.navy.mil/
[3] IEEE Trans Nucl. Sci., Vol 37, No. 6, Dec. 1990, Pages 1961
[4] IEEE Trans Nucl. Sci., Vol 39, No. 6, Dec. 1992, Pages 1600
[5] https://creme96.nrl.navy.mil/cm/AP8.htm